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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/528,188	03/17/2005	Kwangmo Jung	P27608	6693

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EXAMINER	
CHERNYAK, IGOR V	
ART UNIT	PAPER NUMBER
2619	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/528,188	JUNG ET AL.	
	Examiner	Art Unit	
	IGOR V. CHERNYAK	4183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE `3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *06/17/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1-16** are rejected based on broadest interpretation under 35 U.S.C. 102(b) as being anticipated by **Rowett et al. (US 5,991,817)** hereinafter **Rowett.**

3. Regarding to **claim 1, Rowett** discloses a method for integrated processing (a complete router architecture is integrated onto a single silicon chip and includes an internal bus that couples multiple channels to a central processing unit on column 2 line 5 - column 3 line 15) of different network protocols (multiple serial channels and an Ethernet channel receive and transmit data packets that are converted between different network packet protocols by the CPU on column 2 line 5 - column 3 line 15) and multimedia (multimedia on column 22 lines 16-31) (the serial data streams comprise network data packets that are either transmitted or received by the router 12 on Fig.1, 3, 11a, column 9 lines 6 - 43) traffics, comprising the steps of:

(a) converting a packet received from a wide area network (the channels each have an external interface for connecting to different LAN or WAN lines on column 2 line 5 - column 3

line 15) into a common packet on an external network protocol converter (multiple serial channels and an Ethernet channel receive and transmit data packets that are converted between different network packet protocols on column 2 line 5 - column 3 line 15), or converting a packet received from a local area network into a common packet on an internal network protocol converter (a single direct memory access (DMA) controller is coupled to each serial channel and the Ethernet channel and conducts data transfers over the internal router bus on column 2 line 5 - column 3 line 15);

(b) switching said common packet so that said common packet can be switched, bridged, and routed internally (a complete router architecture is integrated onto a single silicon chip and includes an internal bus that couples multiple channels on column 2 line 5 - column 3 line 15) (diagram showing one example of the typical sequence of events conducted by router 12 for routing a data packet between the Ethernet line 88 and one of the serial lines on Fig.1 - 4, column 5 lines 13 - 27);

(c) channelizing to exchange said common packet through dedicated lines according to types of packets (the multi -channel circuitry is configurable to operate with a wider variety of data formats than existing router architectures. In addition, the DMAC 42 conducts a transaction protocol on the internal Bbus 14 that provides more efficient data packet transfers between the multi -channel circuitry 18 and other devices in the router on Fig.1, 11a, column 9 lines 6 - 43);

(d) loading said common packet on a common bus to transmit said common packet to/from a common packet switch (the router 12 includes an internal Bbus 14..... The Bbus 14 is also coupled to a multi -channel circuit 18 which includes an Ethernet channel 40 and multiple serial channels referred to generally as 51. The serial channels 51 are convertible into one or

more time division multiplexed channels for transmitting and receiving data packets on Fig.1, column 4 lines 18 - 52); and

(e) identifying a destination address of data and performing an appropriate protocol conversion on a common packet platform, said common packet platform being able to build free topology through an address translation (the CPU 16 examines a packet header in step 102 for routing information and decides whether the route is known for the data packet in decision step 104..... the CPU 16 in step 108 updates the packet header in DRAM 70, adds the packet to a transmit queue in the DMAC 42, and updates receive statistics. The CPU 16 in step 110 configures the DMAC 42 to transfer the data packet to one of the serial channels 51 on Fig.2 - 4, column 4 line 53 - column 5 line 38).

4. Regarding to **claim 2, Rowett** discloses said step (a) comprises the steps of:

storing temporarily an external or internal network packet entered in a buffer (decision step 234 determines whether the channel associated with the Bbus time slot is ready for a Bbus transfer..... If the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70. The data buffer is located with the data buffer pointer in the buffer descriptor. Decision step 238 continues to write or read from the data buffer on Fig.11a, 20, column 15 line 43 - column 16 line 44);

converting said packet into a common packet format (CPU-intensive task can be handled either as packet data is transferred into memory from an interface, or as data is moved from memory to the interface. This feature provides the router 12 with equal efficiency when translating between protocols that use opposite bit ordering or translating between protocols that use the same bit ordering on Fig.1, 19, column 14 line 52 - column 15 line 42); and

loading said common packet on said common bus to transmit said common packet to said common packet switch (decision step 234 determines whether the channel associated with the Bbus time slot is ready for a Bbus transfer..... If the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70 on Fig.11a, 20, column 15 line 43 - column 16 line 44).

5. Regarding to **claim 3, Rowett** discloses said step (b) comprises the steps of:

storing temporarily said common packet entered in a buffer (if the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70 on Fig.11a, 20, column 15 line 43 - column 16 line 44);

adding a new destination address as desired to a header; and loading said header on said common packet to transmit said header to the new destination (the CPU 16 examines a packet header in step 102 for routing information and decides whether the route is known for the data packet in decision step 104..... the CPU 16 in step 108 updates the packet header in DRAM 70, adds the packet to a transmit queue in the DMAC 42, and updates receive statistics. The CPU 16 in step 110 configures the DMAC 42 to transfer the data packet to one of the serial channels 51 on Fig.2 - 4, column 4 line 53 - column 5 line 38).

6. Regarding to **claim 4, Rowett** discloses said steps (a), (b), (d) and (e) are modularized so that each of them can be operated independently and they can interwork with one another (a complete router architecture is integrated onto a single silicon chip and includes an internal bus that couples multiple channels to a central processing unit. The channels each have an external interface for connecting to different LAN or WAN lines. Multiple serial channels and an Ethernet channel receive and transmit data packets that are converted between different network

packet protocols by the CPU. The serial channels have a novel architecture that allows conversion into one or more time division multiplexed (TDM) channels on Fig.1 - 3, column 2 line 5 - column 3 line 24).

7. Regarding to **claim 5, Rowett** discloses said steps (a), (b), (d) and (e) constitute a plurality of block combinations according to functions (FIG. 1 is a diagram of a router architecture according to the invention and integrated onto a single silicon chip on Fig.1 - 3, column 2 line 5 - column 3 line 24).

8. Regarding to **claim 6, Rowett** discloses said steps (a), (b), (d) and (e) are integrated on a chip so that they can work as a single chip (FIG. 1 is a diagram of a router architecture according to the invention and integrated onto a single silicon chip on Fig.1 - 3, column 2 line 5 - column 3 line 24).

9. Regarding to **claim 7, Rowett** discloses, in order to support a plug and play function, said steps (a), (b), (d) and (e) are designed as an open architecture and external networks or internal networks interwork with said common packet platform (the channels each have an external interface for connecting to different LAN or WAN lines. Multiple serial channels and an Ethernet channel receive and transmit data packets that are converted between different network packet protocols .....The router is integrated onto a single silicon chip reducing manufacturing and assembly costs while at the same time providing an architecture that operates more efficiently with a wider variety of network configurations and network protocols on column 2 line 5 - column 3 line 15).

10. Regarding to **claim 8, Rowett** discloses, in addition to different network protocol conversions through said step (a), an overlay function toward common packet is supported (the

dual PC card controller 54 provides support for two PC card sockets. The controller 54 works between the attached PC card and the external Bbus interface 56 to handle all the control signals…….. A first bus arbitration moves data from the source address into internal storage and the second arbitration deposits DMA data from internal storage onto the external Rbus. Some peripherals such as network and multimedia cards are capable of initiating DMA operations on Fig.29, column 21 line 54 - column 22 line 31).

11. Regarding to **claim 9, Rowett** discloses a system for integrated processing of different network protocols and multimedia traffics, comprising:

a common packet having a header and data to process multi-protocol (the CPU 16 examines a packet header in step 102 for routing information and decides whether the route is known for the data packet in decision step 104…… the CPU 16 in step 108 updates the packet header in DRAM 70, adds the packet to a transmit queue in the DMAC 42, and updates receive statistics. The CPU 16 in step 110 configures the DMAC 42 to transfer the data packet to one of the serial channels 51 on Fig.2 - 4, column 4 line 53 - column 5 line 38);

a common packet switch for switching, bridging, and routing said common packet internally (a complete router architecture is integrated onto a single silicon chip and includes an internal bus that couples multiple channels on column 2 line 5 - column 3 line 15) (diagram showing one example of the typical sequence of events conducted by router 12 for routing a data packet between the Ethernet line 88 and one of the serial lines on Fig.1 - 4, column 5 lines 13 - 27);

a plurality of channels for exchanging said common packet through dedicated lines according to types of packets (the multi -channel circuitry is configurable to operate with a wider

variety of data formats than existing router architectures. In addition, the DMAC 42 conducts a transaction protocol on the internal Bbus 14 that provides more efficient data packet transfers between the multi -channel circuitry 18 and other devices in the router on Fig.1, 11a, column 9 lines 6 - 43);

a common bus for transmitting said common packet to/from said common packet switch (the router 12 includes an internal Bbus 14…… The Bbus 14 is also coupled to a multi - channel circuit 18 which includes an Ethernet channel 40 and multiple serial channels referred to generally as 51. The serial channels 51 are convertible into one or more time division multiplexed channels for transmitting and receiving data packets on Fig.1, column 4 lines 18 - 52);

a common protocol platform able to build free topology through an address translation so as to perform integrated processing of different protocols, different packet formats, and so on (the CPU 16 examines a packet header in step 102 for routing information and decides whether the route is known for the data packet in decision step 104…… the CPU 16 in step 108 updates the packet header in DRAM 70, adds the packet to a transmit queue in the DMAC 42, and updates receive statistics. The CPU 16 in step 110 configures the DMAC 42 to transfer the data packet to one of the serial channels 51 on Fig.2 - 4, column 4 line 53 - column 5 line 38);

an external network protocol converter (multiple serial channels and an Ethernet channel receive and transmit data packets that are converted between different network packet protocols on column 2 line 5 - column 3 line 15) for converting a packet received from a wide area network (the channels each have an external interface for connecting to different LAN or WAN lines on column 2 line 5 - column 3 line 15) into a common packet; and an internal network

protocol converter for converting a packet received from a local area network into a common packet (a single direct memory access (DMA) controller is coupled to each serial channel and the Ethernet channel and conducts data transfers over the internal router bus on column 2 line 5 - column 3 line 15).

12. Regarding to **claim 10, Rowett** discloses said common packet switch comprises:

a buffer part storing temporarily said common packet entered (if the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70 on Fig.11a, 20, column 15 line 43 - column 16 line 44);

a separate channel part based on types of traffic classes (The DMAC 42 provides adjustable bandwidth allocation for each channel. The DMAC 42 can also reduce latency for channels on Fig.11a, column 9 line 66 - column 11 line 19);

a header conversion part where a new destination address as desired is added to a header; and a loader part loading existing data and said header with said new destination address on said common packet (the CPU 16 examines a packet header in step 102 for routing information and decides whether the route is known for the data packet in decision step 104..... the CPU 16 in step 108 updates the packet header in DRAM 70, adds the packet to a transmit queue in the DMAC 42, and updates receive statistics. The CPU 16 in step 110 configures the DMAC 42 to transfer the data packet to one of the serial channels 51 on Fig.2 - 4, column 4 line 53 - column 5 line 38).

13. Regarding to **claim 11, Rowett** discloses said external network protocol converter comprises:

a buffer part storing temporarily an external network packet entered (decision step 234 determines whether the channel associated with the Bbus time slot is ready for a Bbus transfer..... If the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70. The data buffer is located with the data buffer pointer in the buffer descriptor. Decision step 238 continues to write or read from the data buffer on Fig.11a, 20, column 15 line 43 - column 16 line 44);

a conversion part converting said external network packet into said common packet (CPU-intensive task can be handled either as packet data is transferred into memory from an interface, or as data is moved from memory to the interface. This feature provides the router 12 with equal efficiency when translating between protocols that use opposite bit ordering or translating between protocols that use the same bit ordering on Fig.1, 19, column 14 line 52 - column 15 line 42); and

a loader part loading said common packet on said common bus to transmit said common packet to said common packet switch (decision step 234 determines whether the channel associated with the Bbus time slot is ready for a Bbus transfer..... If the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70 on Fig.11a, 20, column 15 line 43 - column 16 line 44).

14. Regarding to **claim 12, Rowett** discloses said internal network protocol converter comprises:

a buffer part storing temporarily an internal network packet entered (if the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70 on Fig.11a, 20, column 15 line 43 - column 16 line 44);

a conversion part converting said internal network packet into said common packet (CPU-intensive task can be handled either as packet data is transferred into memory from an interface, or as data is moved from memory to the interface. This feature provides the router 12 with equal efficiency when translating between protocols that use opposite bit ordering or translating between protocols that use the same bit ordering on Fig.1, 19, column 14 line 52 - column 15 line 42); and

a loader part loading said common packet on said common bus to transmit said common packet to said common packet switch (decision step 234 determines whether the channel associated with the Bbus time slot is ready for a Bbus transfer..... If the channel is ready to either receive or transmit data packets, step 236 begins a DMA to or from a data buffer in memory 70 on Fig.11a, 20, column 15 line 43 - column 16 line 44).

15. Regarding to **claim 13, Rowett** discloses said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are modularized so that each of them can be operated independently and they can interwork with one another (a complete router architecture is integrated onto a single silicon chip and includes an internal bus that couples multiple channels to a central processing unit. The channels each have an external interface for connecting to different LAN or WAN lines. Multiple serial channels and an Ethernet channel receive and transmit data packets that are converted between different network packet protocols by the CPU. The serial channels have a novel architecture that allows conversion into one or more time division multiplexed (TDM) channels on Fig.1 - 3, column 2 line 5 - column 3 line 24).

16. Regarding to **claim 14, Rowett** discloses said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter constitute a plurality of block combinations according to functions (Fig.1 - 3, column 2 line 5 - column 3 line 24).

17. Regarding to **claim 15, Rowett** discloses said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are integrated on a chip so that they can work as a single chip (FIG. 1 is a diagram of a router architecture according to the invention and integrated onto a single silicon chip on Fig.1 - 3, column 2 line 5 - column 3 line 24).

18. Regarding to **claim 16, Rowett** discloses in order to support a plug and play function said common packet, said common bus, said common packet switch, said common packet platform, said external network protocol converter, and said internal network protocol converter are designed as an open architecture, and external networks or internal networks interwork with said common packet platform (column 2 line 5 - column 3 line 15).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to IGOR V. CHERNYAK whose telephone number is (571) 270-1957. The examiner can normally be reached on Monday - Thursday 7:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Len Tran can be reached on 571-272-1184. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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